

REMARKS

Claims 7-12 are pending in the application. Claims 7-9 have been canceled, leaving claims 10-12 for consideration upon entry of the present amendment. Applicant respectfully requests reconsideration in view of the Remarks.

Claims 7-9 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Ogawa (JP 5-335578). Claims 7-9 have been canceled.

Claims 10-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kunii (U.S. 5,412,493) in view of Kawamura (U.S. 5,858,807). For an obviousness rejection to be proper, the Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art; and that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988); *In Re Wilson*, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970); *Amigen v. Chugai Pharmaceuticals Co.*, 927 U.S.P.Q.2d 1016, 1023 (Fed. Cir. 1996).

Claims 10-12 include the following limitation: "said second gate insulating film is made of a material for supplying hydrogen to said semiconductor film and has a smaller film thickness in a region not covered with said gate electrode than that in a region covered with said gate electrode." As recognized by the Examiner Kunii does not teach or suggest that limitation. Instead, the Examiner asserts that Kawamura teaches a silicon nitride insulating film 13 with a smaller film thickness in a region not covered with a gate electrode than a silicon nitride insulating film 8 in a region covered with said gate electrode formed on a silicon oxide insulating film covering a semiconductor region. Applicant respectfully traverses.

The Examiner has misconstrued the claim language. Claims 10-12 require a first gate insulating film, a second gate insulating film and a gate electrode sequentially formed on one major surface of a substrate in that order. Claims 10-12 then recite that the second gate insulating film has a smaller film thickness in a region not covered with the gate electrode than that in a region covered with the gate electrode. As such, the same second gate insulating film is required to be located both under the gate electrode and in a region that is not under the gate electrode. Moreover,

the claim language requires a comparison of the thickness of the second gate insulating film under the gate electrode to the thickness of the same second gate insulating film in a region not covered with the gate electrode.

Kawamura does not and cannot teach or suggest that limitation. The Examiner is using the gate insulating film 8 as the equivalent to the second gate insulating film. The gate insulating film is only located under the gate electrode and has no thickness in a region not covered by the gate electrode. As Figures 1, 2B, and 2C show, the gate insulating film 8 is completely etched away so that it is not located in a region not covered by the gate electrode. Thus, there is no thickness of the gate insulating film 8 in a region not covered with the gate electrode and as such, Kawamura cannot teach or suggest having a smaller film thickness in a region not covered with the gate electrode than that in a region covered with the gate electrode.

Moreover, claims 10-12 require a first gate insulating film, a second gate insulating film and a gate electrode sequentially formed on one major surface of a substrate in that order. As such, the gate insulating film 8 does not equate to the second gate insulating film as suggested by the Examiner; rather, gate insulating film 8 would equate to the first gate insulating film because gate insulating film 8 is sequentially formed before the silicon nitride insulating film 13.

Specifically, Kawamura teaches an amorphous silicon layer 7a and a silicon nitride film 8 are successively deposited on the insulating substrate 1. On the SiN film 8, gate electrode 11 is formed. With the gate electrode 11 being used as a mask, phosphorus is doped into the amorphous silicon layer 7a, thereby turning a portion of the amorphous silicon layer 7a into an n-type amorphous silicon. Thereafter, the entire surface, including the gate electrode, is covered by a silicon nitride film 13.

The SiN film 13 is clearly different from the second gate insulating film of the present invention. Specifically, in Kawamura, after formation of the gate electrode, ion implantation and laser annealing is applied, and then the SiN film 13 is formed. Claims 10-12 require that the second gate insulating film has a smaller film thickness in a region not covered with said gate electrode than that in a region covered with said gate electrode. Because SiN film 13 is the second insulating film applied in Kawamura and because SiN 13 is not covered with the gate electrode, SiN 13 cannot have a smaller film thickness in a region not covered with the gate electrode than

that in a region covered with the gate electrode. Accordingly, Kunii and Kawamura do not teach or suggest all of the limitations of claims 10-12.

In addition, an Examiner cannot establish obviousness by locating references that describe various aspects of a patent applicant's invention without also providing evidence of the motivating force which would have impelled one skilled in the art to do what the patent applicant has done. *Ex parte Levensgood*, 28 U.S.P.Q.2d 1300 (Bd. Pat. App. Int. 1993). The references, when viewed by themselves and not in retrospect, must suggest the invention. *In Re Skoll*, 187 U.S.P.Q. 481 (C.C.P.A. 1975).

Neither Kunii nor Kawamura provide the motivation to combine the two references to reach the claimed invention. Because SiN film 13 is not formed before the doping process, Kawamura is a completely different structure from Kunii and one skilled in the art would not combine the two references. Kawamura does not recognize the idea of preventing intrusion of impurities into the region of the semiconductor film not covered with the gate electrode. Accordingly, there is nothing in Kawamura that suggests changing the thickness of the second gate insulating film between the region under the gate electrode and other regions. In addition, the advantages of the arrangement as claimed in claims 10-12 is explained on page 15, lines 18-23. Specifically, having a larger thickness in the gate electrode region allows the ion doping to be blocked at the gate electrode. In addition, having a smaller thickness in a region not covered by the gate electrode does not block the ion doping into the source and drain region and yet prevents intrusion of impurities or the like, thereby improving reliability of the thin film transistor. Accordingly, because there is nothing in Kunii or Kawamura that would motivate one skilled in the art to combine the two references, Applicant respectfully requests that this rejection be withdrawn.

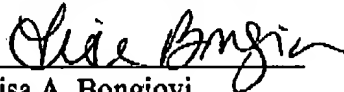
Claims 10-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ogawa (JP 5-335578) in view of Kawamura. The Examiner recognizes that Ogawa does not teach or suggest the following limitation: "said second gate insulating film is made of a material for supplying hydrogen to said semiconductor film and has a smaller film thickness in a region not covered with said gate electrode than that in a region covered with said gate electrode." The Examiner asserts that Kawamura teaches that limitation. As explained above, Kawamura does not teach or suggest that limitation. Thus, for the reasons discussed above, claims 10-12 are allowable

over Ogawa and Kawamura. Applicant respectfully requests that the rejection be withdrawn.

In view of the foregoing, it is respectfully submitted that the instant application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance issued. If the Examiner believes that a telephone conference with Applicant's attorneys would be advantageous to the disposition of this case, the Examiner is cordially requested to telephone the undersigned. In the event the Commissioner of Patents and Trademarks deems additional fees to be due in connection with this application, Applicant's attorney hereby authorizes that such fee be charged to Deposit Account No. 06-1130.

Respectfully submitted,

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